

Exhibit 29

Nick Jones

(He/Him) · 3rd
Director of Engineering at Qualcomm

-  Qualcomm
-  Trinity University

Austin, Texas, United States · [Contact info](#)

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About

Specialties: Functional and formal design verification of ARM A-class microprocessors (middle machine, VMSAv8, CoreSight ETM) with SV/SVA/UVM/C++. Develop and deploy DV tools using Go, Rust, Python, web development (HTML/CSS/JavaScript), SQL, and RabbitMQ.

Activity

800 followers

Nick hasn't posted lately

Nick's recent posts and comments will be displayed here.

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Experience



Qualcomm



Full-time · 2 yrs 1 mo

Austin, Texas, United States

Director of Engineering

Jan 2023 - Present · 3 mos

Principal Engineer

Mar 2021 - Jan 2023 · 1 yr 11 mos



Member Of Technical Staff

NUVIA Inc · Full-time

Nov 2019 - Mar 2021 · 1 yr 5 mos

Austin, Texas Area

NUVIA Inc. was acquired by Qualcomm in March of 2021.

Samsung Austin R&D Center

6 yrs 6 mos

Sr. Staff Verification Engineer

Mar 2017 - Nov 2019 · 2 yrs 9 mos

Austin, Texas

CPU-level functional and formal design verification of ARM V8 architecture using UVM components written in SystemVerilog. Verification Le...see more

Sr. Verification Engineer II

Mar 2014 - Mar 2017 · 3 yrs 1 mo

CPU-level functional and formal design verification of custom design for debug and test (DFD/DFT) features implemented in an ARM V8 a...see more

Sr. Verification Engineer I

Jun 2013 - Mar 2014 · 10 mos

Austin, Texas Area

CPU-level design verification of custom design for debug and test (DFD/DFT) features implemented in an ARM architecture using U...see more



AMD

8 yrs

MTS Systems Design Engineer

Oct 2012 - Jun 2013 · 9 mos

Austin, Texas Area

Cross-functionally leading planning and execution of validation for the APU

in PlayStation 4. This includes producing strategies, plans, execution updates, and risk mitigation for feature and system validation. Working directly with Sony in addressing their needs and concerns in our planning and execution.

MTS Design Engineer

Jun 2011 - Oct 2012 · 1 yr 5 mos

Austin, Texas Area

Developed SystemVerilog and C++ test benches, checkers, monitors, SystemVerilog Assertions (SVA), and test cases against Verilog instances of DFX IP in a parameterized, random environment. Also partnered with the Software Tools teams to enable leveraging hardware features for debugging purposes. Started some work in using UVM 1.1 on a new test bench.

MTS Systems Design Engineer

Nov 2010 - Jun 2011 · 8 mos

Austin, Texas Area

Test planning and technical leadership of a team in executing emulation test plans prior to silicon tape-out.

Show all 7 experiences →



Student Systems Administrator

Trinity University

Aug 2004 - May 2005 · 10 mos

Education



Trinity University

BS, Engineering Science with a specialty in Electrical Engineering

2001 - 2005

Lakeridge High School

Skills

Debugging



Endorsed by Jason Doege and 27 others who are highly skilled at this



Endorsed by 2 colleagues at Qualcomm



56 endorsements

SystemVerilog



Endorsed by 17 colleagues at AMD



19 endorsements

X86



Endorsed by Vaseekaran Rajagopal and 2 others who are highly skilled at this



Endorsed by 23 colleagues at AMD



24 endorsements

Show all 49 skills →

Recommendations

Received

Given



Scott Matlock · 3rd

Lead Debugger for System level issues on 5G Baseband and Radio products
February 21, 2014, Scott managed Nick directly

I was Nick's manager for four years while Nick was in the Customer Debug group. Nick was one of the best engineers in all of AMD and consistently performed well above his title. Nick has an exceptional grasp of system level concepts including computer H/W, BIOS, OS, Application S/W and H/W...



James (JT) Longino · 3rd

Verification Engineer

July 19, 2013, James (JT) worked with Nick on the same team

Nick is a stunningly capable engineer with a broad understanding of both hardware and software. He brings an insatiable curiosity and ever-growing toolbox to whatever problem he runs across, but has enough business sense to not just wander off looking for something cool to do. ...

Publications

Leveraging LevelDB for Unit Level Display of Top Level Stimulus in UVM

Leveraging LevelDB for Unit-Level Replay of Top-Level Stimulus in UVM

SNUG Austin · Jan 1, 2016

[Show publication ↗](#)

Also presented at DVClub Austin (2018) and DVClub Europe (2019).

Courses**ARM - ARM V8 Architecture**

Associated with Samsung Austin R&D Center

Cadence - UVM 1.1

Associated with Samsung Austin R&D Center

Coursera - Stanford Cryptography I[Show all 5 courses →](#)**Honors & awards****AMD Spotlight Award**

Jan 2011

Scan dump analysis engine (Scan View)

AMD Spotlight Award

Jan 2010

Creation of an automation and characterization platform

AMD Spotlight Award

Jan 2010

Barracuda bring-up efforts

[Show all 5 honors & awards →](#)**Languages****English**

Native or bilingual proficiency

Korean

Limited working proficiency

Interests

Top Voices

Companies

Groups

Schools



Bill Gates

Co-chair, Bill & Melinda Gates Foundation

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Director Engineering, CPU Physical Design at Qualcomm (Nuvia)

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Principal Engineer at Qualcomm

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Engineer at Qualcomm

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Principal Engineer at Qualcomm - NUVIA

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Business Development Manager

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Marketing and Communications Coordinator at Robins Kaplan LLP

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Partner at Robins Kaplan LLP

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Senior A/V Engineer, Trial Consultant and Multimedia Expert at Robins Kaplan LLP

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